ABSTRACT

DEVICE FOR A HIGH SPEED RECEIVER

The present invention is related to a device comprising, between a differential pair of inputs, a differential pre-amplifier (HPA1, HPA2), an offset-reducing block (ORB) cascaded with said differential pre-amplifier (HPA1, HPA2) and arranged for reducing the offset generated by said differential pre-amplifier, and a buffering block (BB) in series with said offset-reducing block (ORB) and arranged for amplifying and buffering the output voltage of said offset-reducing block.

(Figure 2)